BOX AFTER FINAL
EXPEDITED PROCEDURE
740756-1930

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT application of	)	
Shunpei YAMAZAKI et al.	)	
Serial No. 09/239,948	)	Art Unit: 2811
Filed: January 29, 1999	)	Examiner: G. Munson
For: A MEMORY DEVICE HAVING A FLOATING GATE (AS AMENDED)	)	

21/E(X)
FJONES
12-7-01

AMENDMENT AFTER FINAL UNDER 37 C.F.R. 1.116

Commissioner of Patents
Washington, D.C. 20231

November 5, 2001

Dear Sir:

In response to the Examiner's Final Office Action mailed July 5, 2001, please consider the following amendments and remarks in connection with the above-identified application.

IN THE ABSTRACT:

Please change the Abstract to read as follows:

E1

A semiconductor memory device including a first memory having a first floating gate formed over a semiconductor substrate, a first control gate formed over and insulated from the first floating gate, a first impurity region and a second impurity region formed within the semiconductor substrate, wherein the first impurity region is deeper than the second impurity region, and a second memory having a second floating gate formed over the semiconductor substrate, a second control gate formed over and insulated from the second floating gate, the first impurity region, and a third impurity region formed within said semiconductor substrate, wherein the first impurity region is deeper than said third impurity region, and a pair of wirings formed on and in electrical contact with the second and third impurity regions, respectively. In one embodiment, the pair of wirings may function as a bit line.